MIS μ-calorimeters arrays: an alternative to IXO/XMS TES/Squids baseline

Abdelkader Aliane[a], J.L. Sauvageot[b], X. de la Broïse[c], C. Pigot[b], J. Martignac[b], E. Grémion[c], V. Szeflinski[b], J. Goupy[a], and P. Agnese[a]

[a]Commissariat à l'Energie Atomique, CENG Grenoble, France;
[b]CEA, DSM/IRFU/Service d'Astrophysique, 91191 Gif/Yvette Cedex, France
[c]CEA, DSM/IRFU/SEDI, 91191 Gif/Yvette Cedex, France

ABSTRACT

The IXO/XMS instrument baseline is an array of TES sensors. Alternatively, we are now developing a μ-calorimeter array based on Silicon doped sensors. Our strength stands in a very low power consumption at 50 mK, allowing more than 4000 readout channels in the limited power budget of the IXO/XMS cryostat, for a Field of View as large as 6'x6' square while keeping the same spectral resolution. In parallel, we develop the cold (2-4K) frontend electronics based on High Electron Mobility Transistors (GaAlAs/GaAs) and SiGe ASIC electronics to readout, amplify and multiplex the signals. We present the status of our development and our current design study.

Keywords: X-rays, IXO, μcalorimeters array, Metal-Insulator Sensors, Cold Electronics

1. INTRODUCTION

Since the advent of CCDs twenty years ago, the astrophysical community awaits for large X-ray calorimeter arrays. Most of laboratories developing μcalorimeters based, nowadays, their technological choices onto Transition Edge Sensors (TES) and SQUIDs. Since we have successfully developed the Herschel/PACS instrument based on Metal-Insulator Sensors (MIS), we have started some years ago an evolution of these IR bolometers toward MIS X-ray μcalorimeters. In contrast with the "hand made" 30 pixels of the SUZAKU/XRS detector, our idea was to use silicon-only collective technologies to realize the full 32x32 sensor array. In addition, thanks to a collaboration with the Laboratoire de Photonique et Nanostructure (LPN), we have an High Electron Mobility Transistor (HEMT) able to work at low temperature as a first electronic stage. Based on these building blocks, we started a development of large MIS μcalorimeters array.

In an early paper,[Aliane et al.(2008)] we have extensively described most of our choices in the pixel design including the doped silicon thermometer fabrication and the collective indium bump hybridization process of the Tantalum absorber. In a subsequent paper[Szeflinski et al. (2009)] we have described our thermal measurement of the hybridization optimization. Here, we will present our first dynamical measurement on our pixels, the design and status of the cold frontend electronic and the system study to fit in the XMS instrument on board IXO mission. The measurements presented here come from our very first 8x8 batch. Anyway, we foresee a complete Focal Plane Assembly (FPA) made of four quadrants of 32x32 $500\mu m$ μ-pixels.

2. THERMAL CHARACTERIZATION OF OUR PIXEL

2.1 The thermal conductance to the cold bath

In order to extract the thermal properties of our pixel, we have developed a specific pixel with two resistors-thermometers onto the freed silicon membrane. The figure 1, on the left, give a schematic view of this pixel.

The thermal conductance of our pixel to the cold bath was measured using this bi-sensor pixel. We inject continuously a given power in one resistor, and use the other one to determine the achieved temperature in steady state. This allows us to directly obtain the conductance to the cold bath. The figure 1 shows these measurements. Fitting the data with the relation $P = K \times (T^4 - T_0^4)$, we found a thermal conductance $G = \frac{\partial P}{\partial T} = 4K \times T^3 = 7.7\ 10^{-13} W/K$ at 50mK.

Send correspondence to J.L.S. email: jean-luc.sauvageot@cea.fr

Space Telescopes and Instrumentation 2010: Ultraviolet to Gamma Ray,
edited by Monique Arnaud, Stephen S. Murray, Tadayuki Takahashi, Proc. of SPIE Vol. 7732,
77321O · © 2010 SPIE · CCC code: 0277-786X/10/$18 · doi: 10.1117/12.856878

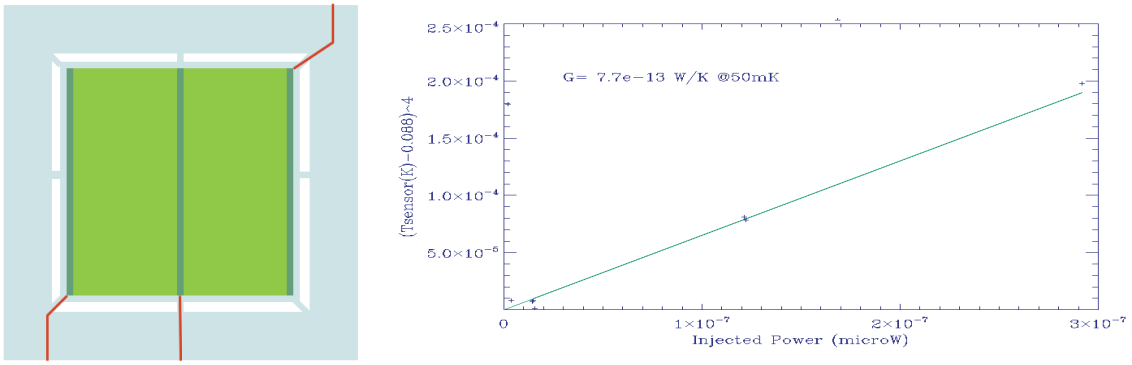

Figure 1. On the left, schematic view of the pixel with the two thermometers (in green) onto the suspended Silicon membrane. Dark green rectangles are the region of the contact pads. The red lines are Superconducting output lines. On the right, measurement of the Thermal impedance of the bi-sensor pixel to the cold bath.

2.2 Heat capacity measurement of the pixel

Once we have measured the thermal conductance to the cold bath, we can estimate the heat capacity of the sensor. Using a lock-in amplifier synchronized with a pulse injected onto one resistor-sensor, we were able to measure the decay time of the temperature at various cold bath temperatures. This decay time τ is directly linked to the sensor heat capacity through equation $\tau = C/G$, where C is the heat capacity. Using the thermal conductance found, we have estimated the heat capacity of our sensor to $C_{Sensor} = 1.37\ 10^{-14} J/K$ at 60mK. We have tried to fit the data with a function like $C(T) = \frac{\alpha}{T} + \frac{\beta}{T^3}$, representing the electronic and phonon contributions (see fig. 2). The sensor does not seem to have any linear dependency with the temperature but only a cubic one as if there were very few electronic contribution. After adding the theoretical heat capacity foreseen with our tantalum absorber, we end up with a heat capacity of the whole pixel of $C_{pixel} \simeq 3\ 10^{-14} J/K$. If our frontend electronic has a noise contribution matching the sensor Johnson noise, these numbers are really encouraging in view of our goal in spectral resolution of 2-3 eV at 6keV.

3. FRONTEND ELECTRONIC DESIGN

The main constraints in the frontend electronic design come from the high impedance of the sensors ($R_{Sensor} \sim 1M\Omega$), a fast signal (risetime$\sim 10\mu$s) and limited power at the 50mK temperature ($P_{tot} < 1\mu W$@50mK) stage. This imposes an amplifying and multiplexing electronics close to the detectors. This electronics must :

- operate at low temperature to be close the sensors,
- have very high input impedance matched to the detector one,
- have a low input capacitance not to limit the required frequency bandwidth,
- have a ultra low noise, down to low frequency, matching the Johnson noise of the sensor,
- dissipate as less as possible on the first stage of the cryo-cooler.

These very sharp requirements are achievable thanks to the High Electron Mobility Transistors (HEMT). Recent HEMTs specifically developed to our needs by LPN present excellent tradeoffs in noise versus entrance capacitance with a negligible input current. The main characteristics of these devices can be summarized as following: Input capacitance $\sim 5 - 6pF$, Noise$\sim 2nV/\sqrt{Hz}$ at 1kHz, typical consumption $\sim 50\mu W$ ($80\mu W$ including 30Ω charge).

In addition, the BiCMOS SiGe technology by Austria MicroSystems (AMS) works at temperature as low as 4 K (even less for MOS transistors), its noise (Noise $\sim 0.5nV/\sqrt{Hz}$ at 1kHz) and gain performances are still

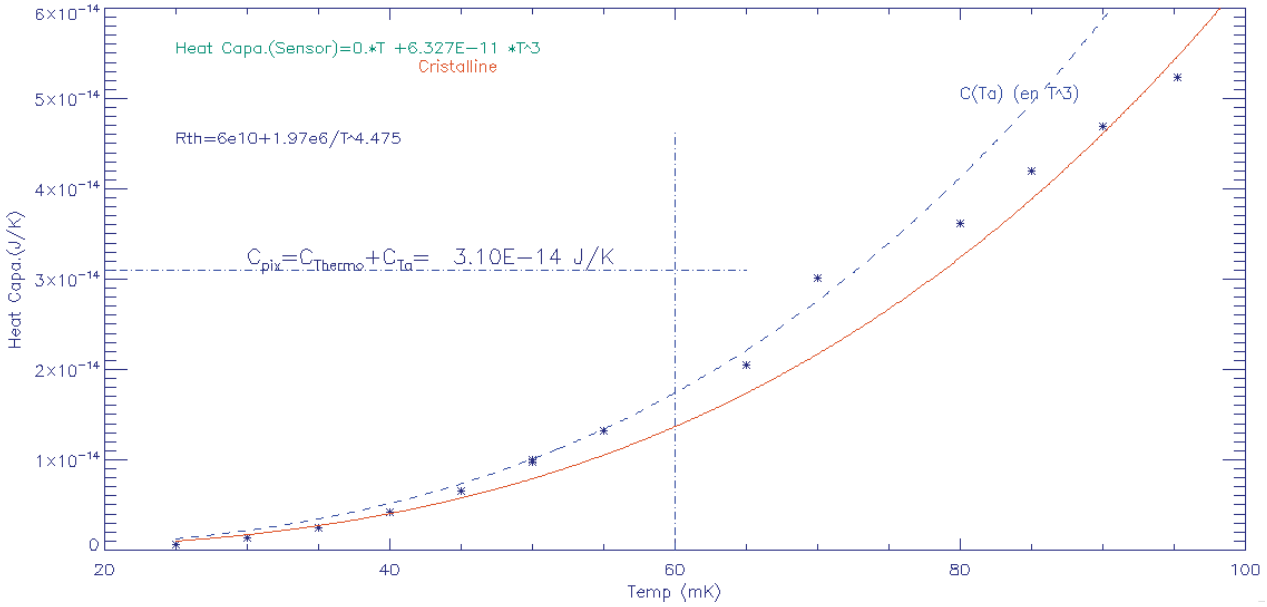

Figure 2. Heat Capacity of the sensor. Red line is the best fit over the full 25-100mK range ($C_{Sensor} \simeq 1.4\ 10^{-14} J/K$ @$60mK$). Dashed line represents the theoretic heat capacity of the Tantalum absorber ($C_{Ta} \simeq 1.7\ 10^{-14} J/K$ @$60mK$). Once both contribution have been added, we found a total heat capacity of the pixel to be around $3.1\ 10^{-14}\ J/K$@$60mK$.

good at these temperatures, its design kit is large, and allow the design of complex circuits. And, last but not least, this set of technology is routinely used in our laboratory, and some parts have been adapted to be radiation tolerant.

3.1 FrontEnd CryoElectronics Architecture

To fit inside the power budget, while minimizing the noise and keeping enough bandpass, we end up with a four stages scheme (see fig. 3):

- The detector biasing (simple resistors) at 300 mK.
- The (high input impedance) HEMT input stage at 2.5 K.
- The multiplexing and power commuting SiGe ASIC stage at 2.5 K.
- The amplifying SiGe ASIC stage at 15 K.

3.2 Power Budget at different stages of the cryo-cooler

The architecture is not only driven by electronics requirements. It takes also into account the thermal dissipation and connection constraints. The dissipation has been optimised according to the available cold power at each stage (see fig. 4).

For the input stages, two options are developed in parallel: The commuted currents option, which is our baseline and currently tested and the commuted charges option. This option should reduce the power budget to markedly less than $0.5\mu W$ at 2.5 K, and to $\sim 60\mu W$ at 15K. But its noise properties and crosstalk level are difficult to predict, and so should be measured.

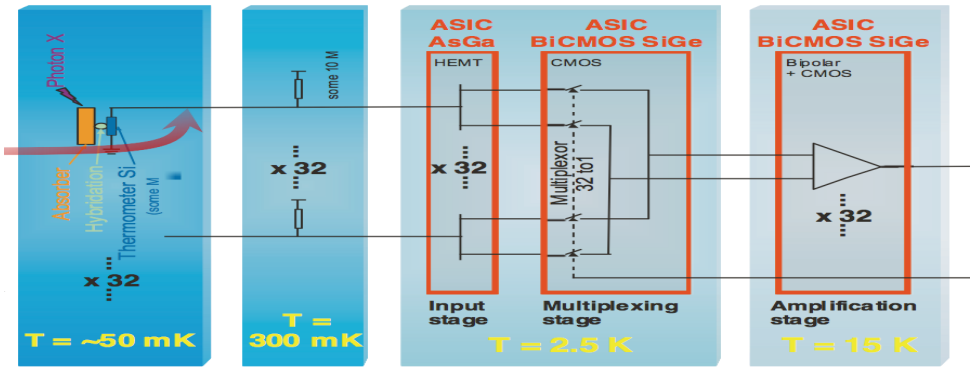

Figure 3. Schematic of our four stages FrontEnd CryoElectronics. The 300mK stage hold the polarization resistors; At 2.5K we put the first electronic input stage (HEMTs), and the multiplexing SiGe ASIC. Finally, at 15K, the amplifier stage.

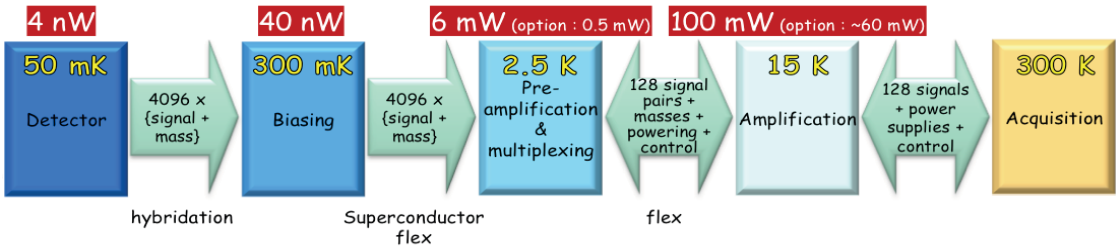

Figure 4. Foreseen power dissipation of the all stages of the FrontEnd Electronics at the different temperatures levels.

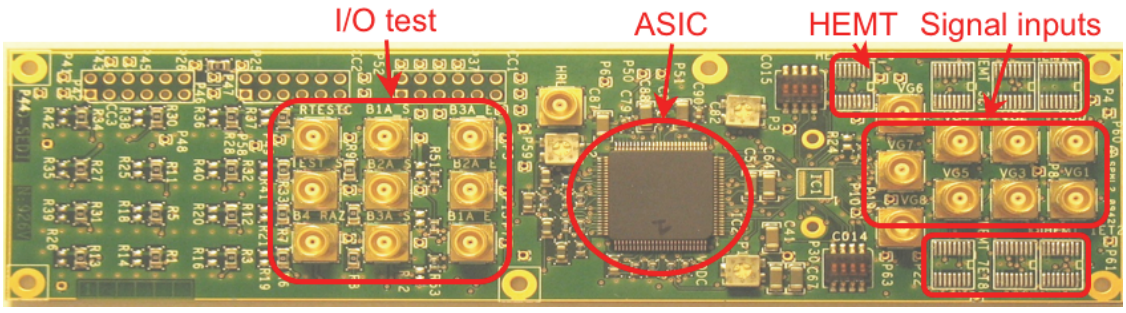

Figure 5. Test board with HEMTs and second stage SiGe ASIC routinely tested at 4K

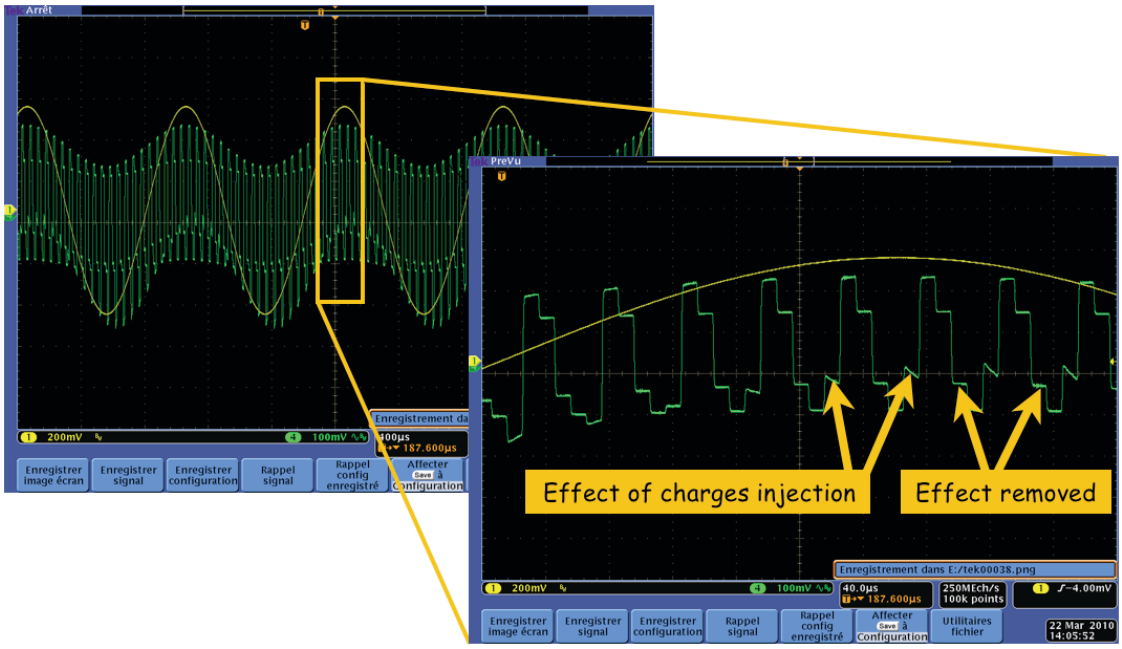

Figure 6. This figure display a 100 kHz 4-channels multiplexed signal with two pixels using the anti-charge injection system. Notice the flat level achieved thanks to the anti-injection system.

3.3 First Results

We have developed a board to test easily this electronic in an Helium dewar (see fig. 5). The ASICs developed were foreseen to be testable independently at all their functionality levels. In this sense, they are more demonstration toolboxes than real optimized chain. All the digital functions, including a serial link, registers, a sequencer and switches are fully operational at 4K. Frequency performances have been measured. The bandwidth measurement (i.e. the input signal bandwidth and the multiplexed signal bandwidth) comply with the requirements as expected from the design and simulations. Commutation and multiplexing performances have been checked up to 1MHz. Very first noise performances have been obtain recently, demonstrating a noise already at the level of $\sim 1.5nV/\sqrt{Hz}$ at 10kHz which should decrease in the second ASIC generation when the extra outputs used for testing will be suppressed.

In order to reduce the power consumption at low temerature, we restrict the power to the only operating input stage which is being readout. Such a commutation of the input stage induces injection on the detector, perturbating the sensor. We have, thus, designed an anti-charge injection system to avoid this problem (see fig.6). This system works properly and the remaining unavoidable transients are too short to be detected at the output of the electronics.

In conclusion, all the performances fulfil the requirements or are very close to do so: frequency bandwidth, commutation and multiplexing speed and signal shape, anti-charge injection system, power dissipation. The electronic architecture is thus practically validated. Tests in cryostat connected to a detector at 50mK will be done soon.

The next steps will be an SiGe ASIC with 33 inputs channels, commutation and amplification functions separated in two ASICs, including the baseline option(commuted currents) and the commuted charges option (still to be tested).

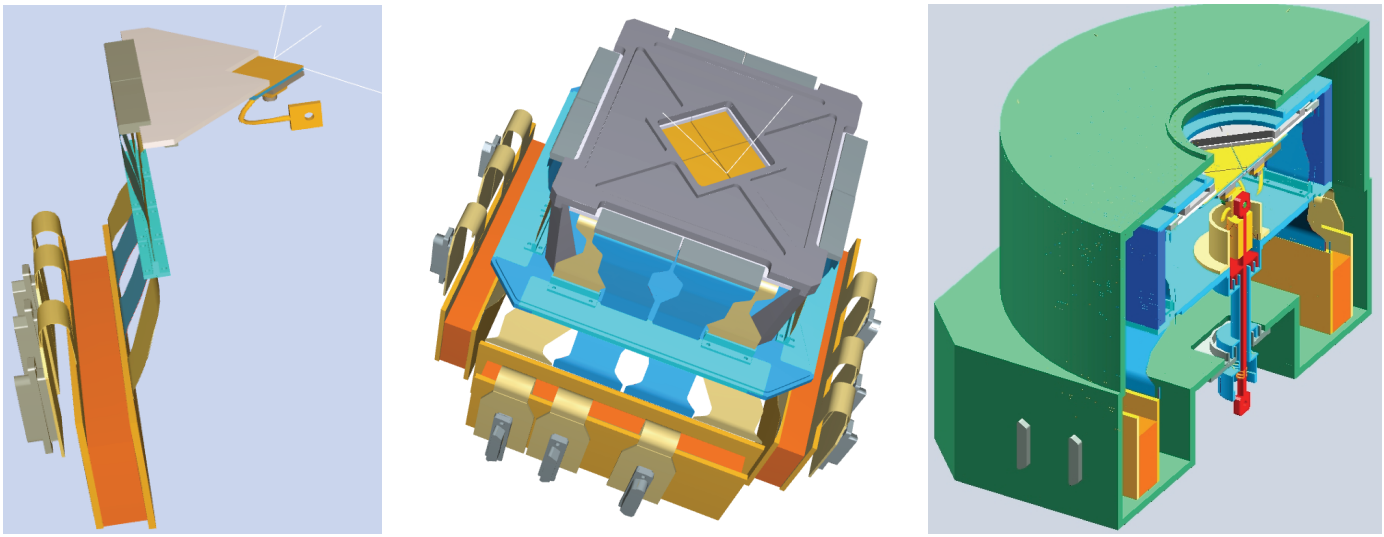

Figure 7. On the left, a full quadrant of 32x32 pixels (in color gold) with, in grey, the fanout circuit, the flexes and, in orange, the FrontEnd CryoElectronic. In the middle, an open view of the 4 quadrants mosaic constituting the Focal Plane Assembly (FPA). On the left, cross-section of the FPA in the inner cryostat. One can see, in light blue, the 300 mK box holding the four 32x32 detectors, in yellow. The green box is the 2.5K one. The red part is the 50mK strap.

4. MECHANICAL AND THERMAL DESIGN

In last spring 2009, we have answered the "Declaration of Interest" emitted by ESA for the IXO instruments and consequently, started a system analysis that we will present in this section. The main driver of this study is to inherit of what we learn with the Herschel/PACS instrument at 300mK using Kevlar wires as a thermal insulation suspension of the 300mK box from the 4K cryostat.

In addition, from the beginning of this design, we have in mind to minimize as much as possible single point failure, while, in the same time, insuring testability of main parts of the system. We decomposed the FPA in four quadrants. Each quadrant with its associated electronics should be fully tested prior to final mounting. The figure 7, on the left, shows a schematic view of a quadrant. It is composed of a 32x32 detector matrix (gold color, at 50mK) with a fanout circuit (in white, at 300mK), a flex from 300mK up to 2.5K, the associated frontend electronics (in orange). In the middle, we present an open view of the 4 quadrants mosaic constituting the Focal Plane Assembly (FPA) and, on the right, a view of the complete FPA. One can see, in red, the 50mK straps insulated from the 300mK through the use of Kevlar wires. The 300mK box is also suspended to the 2.5K box with Kevlar wires. A similar system designed for the SPICA/Safari instrument has been realized and successfully passed first vibration tests (see the paper 7741-103 at this conference by J. Martignac for a complete description of theses results).

5. OUTPUT AND CROSSTALK OF SIGNALS IN A 32X32 MATRIX ARRAY

In view of our next batch of a 32x32 pixel array, we have deeply investigated the way to output two wires per pixel on a 32x32 matrix letting two sides free of wire (to have a matrix 2-sides abutting). The silicon walls between our sensors are foreseen to be around 140 μm, a pitch of $4\mu m$ for the wires is achievable. This allows at most 32-33 wires on each wall. For crosstalk reasons, we also wanted to have all the wiring on one level. We have written a specific optimisation code to take into account all of these constraints while minimizing the mean foreseen crosstalk between pixels. We present in the fig 8 an illustration of such a solution.

6. PERSPECTIVES & CONCLUSION

At this level of our development, we have achieved a major cornerstone with this first version of our cold frontend electronics. Most laboratories that were developing MIS sensors stopped their developments since they

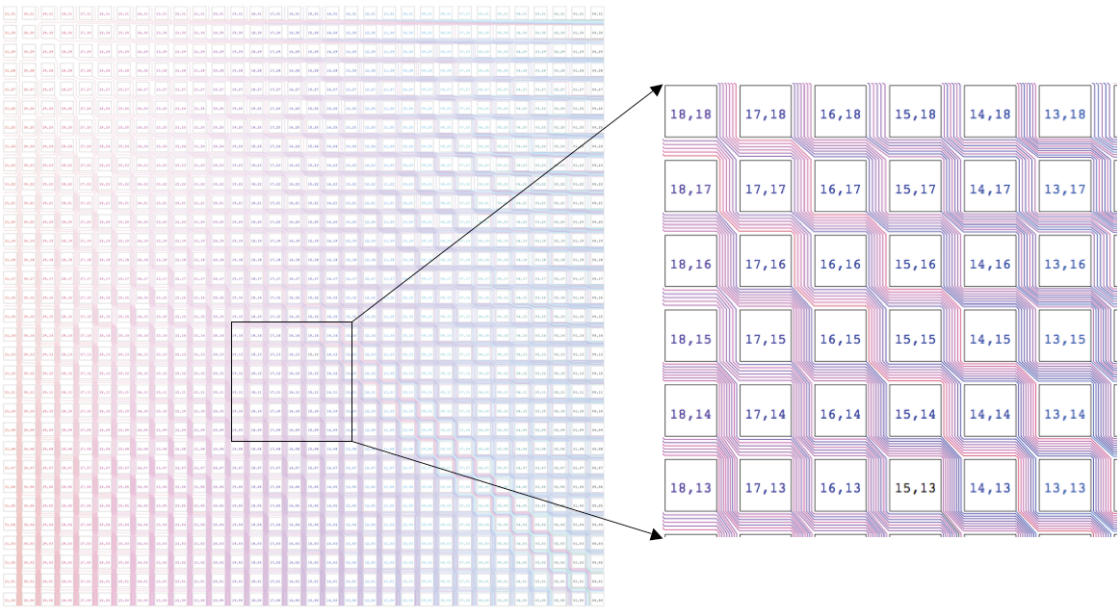

Figure 8. Realization of a 32x32 routing scheme on one plan with at most 16 pairs of wires on each wall with mean crosstalk between pixels minimized. Notice that this routing allow to have a 32x32 matrix 2-side butable with only one layer of wires.

were foreseeing no solution for this cold frontend electronic in the tight power budget allowed in cryogenic space mission.

We are still missing the first X-ray measurement, but each building block looks in a pretty good shape. We plan to test our first array with this electronic in summer. In the following year, we will build our first 32x32 matrix and its associated electronics able to operate the full matrix. This will be our demonstrator for the IXO/XMS instrument.

ACKNOWLEDGMENTS

This work is funded by Commissariat à l'Energie Atomique and by the Centre National d'Etudes Spatiales.

REFERENCES

[Aliane et al.(2008)] Aliane, A., Agnese, P., Pigot, C., Sauvageot, J.-L., de Moro, F., Ribot, H., Gasse, A., Szeflinski, V. and Gobil, Y., 2008, Nuclear Instruments and Methods in Physics Research A, 594, p210

[Szeflinski et al. (2009)] Szeflinski, V., Aliane, A., de Moro, F. and Pigot, C., Sauvageot, J.-L., Agnèse, P., Gasse, A. , Ribot, H., Gremion, E. ,de la Broise, X. and Navick, X. F.,2009, Nuclear Instruments and Methods in Physics Research A, 610, p345